MPPA® MANYCORE is a family of programmable manycore processors, well-suited for compute intensive and embedded applications enabling unique power efficiency.

It relies on KALRAY’s proprietary Multi-Purpose Processor Architecture, a core technology made up of leading-edge components, resulting from many years of research, enabling application scaling.

Product family overview

The MPPA® (Multi-Purpose Processor Array) solution is built around a family of programmable silicon devices implementing KALRAY’s core technology.

The MPPA® MANYCORE chips feature up to one thousand processors on a single die. They come in various configurations to best match customer applications and requirements (see Table 1). All MPPA® MANYCORE products feature voltage and frequency scaling, allowing optimal power dissipation and computing performance.

<table>
<thead>
<tr>
<th>Core Generation</th>
<th>Number of Processing Cores</th>
<th>GFLOPS/W</th>
<th>GOPS/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>Andey</td>
<td>256</td>
<td>25</td>
<td>75</td>
</tr>
<tr>
<td>Bostan (2014)</td>
<td>256</td>
<td>50</td>
<td>80</td>
</tr>
<tr>
<td>Coolidge (2015)</td>
<td>64/256/1024</td>
<td>75</td>
<td>115</td>
</tr>
</tbody>
</table>

Table 1 – MPPA® MANYCORE Roadmap

The MPPA® MANYCORE is composed of an array of clusters connected through a high-speed Network-on-Chip (NoC). Each cluster contains 16 processing cores, a system core and a shared memory.

The MPPA® MANYCORE family implements state of the art power management techniques as well as innovative patented schemes to reach unprecedented power dissipation over computing power efficiency ratios.

Multiple MPPA® processors can be connected together at board level through a NoC extension, thus enabling virtually any size of processor arrays.

Target applications

The MPPA® MANYCORE processor family combines high performance capabilities with low power dissipation, making it a perfect fit for power efficient and embedded applications:

- **Image and Audio processing:** HD encoding, broadcasting, video surveillance, augmented reality
- **Signal processing:** Radar, telecom, medical
- **Intensive Computing:** Oil & Gas, finance, video live streaming, numerical simulation, Bio Sciences
- **Control Command:** Aeronautics, industrial automation
- **Telecom:** Routers, cryptography, software defined radio, base station

Features

- From 64 to 1024 cores delivering up to 8 TOPS or 5 TFLOPS
- Best Processing Power / Power Consumption ratio
- C/C++/Fortran based parallel programming solution
- Very Long Instruction Word (VLIW) core
- IEEE-754 single and double precision Floating Point Unit (FPU)
- High speed Network on Chip bandwidth
- Advanced NoC Quality of Service enabling predictable data transfer time
- High speed interfaces, Ethernet, DDR3, PCIe Gen3, NoCX
- Low latency processing

Key benefits

- 5 to 10x performance/power ratio compared to other computing solutions
- 10x improvement in power consumption for typical applications
- Development time reduced by a factor of 2 to 4 compared to FPGA or ASIC designs
- Quick product upgrade through software development

The MPPA® MANYCORE processor achieves this by combining:

- Advanced Silicon technology
- The computing power of the Kalray core
- Numerous simple processors on the same die, running at moderate frequency and linked by a high speed network
- High speed connections to the external world
- Complete software development tools
MPPA®-256 Architecture overview

The MPPA®-256 is the first processor of KALRAY MPPA processor and is composed by an array of 16 clusters and 4 I/O subsystems, themselves connected by two NoCs.

Core architecture

The MPPA® core is a 32-bit Very Long Instruction Word (VLIW) processor made of:

- One Branch/Control Unit
- Two Arithmetic Logic Units
- One Load/Store Unit including simplified ALU
- One Multiply-Accumulate (MAC) / FPU including a simplified ALU
- Standard IEEE 754-2008 FPU with advanced Fused Multiply-Add (FMA) and dot product operators
- One Memory Management Unit (MMU)

This enables to execute up to five 32bit RISC like integer operations every clock cycle.

Compute Cluster

Each compute cluster is composed of:

- 16 identical cores with private FPU and MMU
- Dynamic Voltage and Frequency Scaling (DVFS) and Dynamic Power Switch off (DPS) support
- 1 system core with private FPU and MMU
- An instruction and data L1-cache per core
- 1 smart Direct Memory Access (DMA)
- A shared memory
- 1 Debug Support Unit

The cores are connected to a multibank memory enabling low latency access or bank private access depending on the configuration.

Network on Chip

The NoC is a 2D-wrapped-around torus structure providing a full duplex bandwidth up to 3.2 GB/s between each adjacent cluster. The NoC implements a Quality of Service mechanism, thus guaranteeing predictable latencies for all data transfers.

Interfaces

The MPPA MANYCORE processor communicates with the external devices through I/O subsystems located at the periphery of the NoC. The I/O subsystems implement various standard interfaces.

Here below the description of MPPA-256 interfaces:

- Two DDR3 channels
  Each channel is 64-bit with optional ECC and delivers up to 12.8GB/s.
- Two PCIe Gen3 X8
  Each interface embeds an advanced DMA with scatter/gather supports providing efficient data transfer as PCIe Bus master.
- Two smart Ethernet Controllers
  Each controller can be configured to provide 4x1GbE, 4x10GbE or 1x40GbE interface.
- Universal Static Memory Controller
  This controller enables to connect up five external devices like NAND/NOR Flash, serial Flash and asynchronous SRAM memories
- Two banks of 64 General Purpose I/Os
  Each bank can be configured in PWM, UARTs, SPI or I2C.
  These banks can work also in Direct Network Access mode, providing a very low latency interface to directly stream data from/to the processing array.
- NoC eXpress interfaces (NoCX)
  Providing an aggregate bandwidth of 40Gb/s, the NoCX enables to easily scale the number of cores by connecting multiple MPPA MANYCORE processors on the same board. The NoCX is also an efficient way to couple the MPPA with an external FPGA used as a co-processor or interface bridge.

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